Next-generation radiation-hardened computer enable previously impossible military small satellites to deep space missions

The advances in space demand next generation of space data and signal processing requirements High speed computers enable on-board image processing capability reduce the amount of bandwidth required to downlink the enormous images associated with emerging sensor developments. Onboard processing allows a complete image to be down linked directly to the battlefield commander, providing the operational forces with real-time imagery. This would reduce the dependence on the numerous ground stations.

An additional benefit of the high-performance space computer is the capacity to provide the user with autonomous mission operation, going beyond spacecraft control to increasingly independent information gathering, multispectral and hyperspectral data analysis, and data dissemination.

The increased satellite autonomy and processing capability will dramatically improve satellite system performance and decrease the support infrastructure while providing needed information directly to end users.

However, Deep-space and long-duration missions, where both crew members and spacecraft no longer benefit from the protection of Earth’s magnetic fields, are considered high risk for adverse radiation impacts. Long term exposure of astronauts to radiation is problematic and the effect that space radiation has on spacecraft electronics and software is

equally challenging. The computers in space must meet the radiation-hardness requirements of the severest space environment.

Ionizing radiation takes a few forms: Alpha, beta, and neutron particles, and gamma and X-rays. The ability of Radiation to affect electronic devices depends on its ability to penetrate the electronic equipment and then to penetrate the packages with semiconductor devices in them. Usually it will be beta and gamma radiation that will have this ability; alpha particles will usually be stopped by outer packaging very easily.

The common quality that is measured in Radiation is its ability to ionise materials. In semiconductors this ionising radiation can have two major effects: one is to produce electron-hole pairs which can create “soft” errors (errors in operation but not permanent damage) and, if the radiation is sufficient, permanent damage by creating large numbers of charges with sufficient energy to be injected into Silicon dioxide regions (where they stick) and change a transistors characteristics. Such high levels of radiation can also disrupt the crystal lattice and damage the transistors in that way.

Normal semiconductor devices such as those in a typical computer would have sufficient soft errors at relatively low levels of radiation to render the computer unusable though not necessarily cause permanent damage. However, it is possible to make semiconductor devices that are very resilient to radiation – at least for a period of time. This involves different processing and careful design and, as a result, they are not cheap to make. Typically they will use a silicon-on-insulator process and complete computers can be made (and are made for military applications) that can withstand around 1 megarad, which would be lethal to a human.

U.S. government space researchers want industry to develop a next-generation radiation-hardened, general-purpose, multi-core processor within the next four years to meet on-board computing needs of future manned spacecraft and space robots.

Today’s radiation-hardened space processors typically are single-processor systems based on existing commercial or military computers. they operate at maximum required throughput, fault tolerance, and power levels. Air Force and NASA space experts, however, say they anticipate future missions that will require an increase in throughput and wider variations in throughput, fault tolerance, and power levels.

To do this they need a new space processor design that will provide orders of magnitude improvement in performance and performance-to-power ratio as well as the ability dynamically to set the power-throughput-fault tolerance operating point.

A BAE Systems develops RAD5545 Next-generation single-board space computer

BAE Systems, a world leader in radiation-hardened computers and processors for satellites and spacecraft, today announced a new generation of its flagship space computer that combines fast performance and extreme resiliency to enable previously impossible missions in the harsh environment of space.

The new RAD5545TM single-board computer (SBC) provides next-generation spacecraft with the high-performance onboard processing capacity needed to support future space missions – from weather and planetary exploration to communications, surveillance, tracking, and national security missions. The RAD5545 SBC delivers exponential improvements in size, speed, and power-efficiency over its proven predecessor, the RAD750® SBC.

“The RAD5545 SBC is the next step in the evolution of space computers. It’s the most technologically advanced radiation-hardened, general-purpose processor for space applications,” said Dave Rea, director of On-board Processing and Advanced Technology at BAE Systems.

A single RAD5545 SBC replaces multiple cards on previous generations of spacecraft. It combines high performance, large amounts of memory, and fast throughput to improve spacecraft capability, efficiency, and mission performance. With its improved computational throughput, storage, and bandwidth, it will provide spacecraft with the ability to conduct new missions, including those requiring encryption processing, multiple operating systems, ultra high-resolution image processing, autonomous operation, and simultaneous support for multiple payloads – missions that were impossible with previous single-board computers.

The RAD5545 SBC is produced at the company’s facility in Manassas, Virginia. The facility is a U.S. Department of Defense Category 1A Microelectronics Trusted Source.

BAE Systems’ radiation-hardened electronics have been onboard satellites and spacecraft for almost 30 years, delivering long-lasting computing power in extreme environmental conditions. The company has provided more than 900 computers on over 300 satellites, and has provided the computers that power key national space assets, including some that are hundreds of millions of miles away from Earth.

Air Force, NASA to develop radiation-hardened ARM processor for next-generation space computing

Officials of the NASA Goddard Space Flight Center in Greenbelt, Md., issued the final solicitation Monday for the

High Performance Spaceflight Computing (HPSC) Processor Chiplet program for NASA and U.S. Air Force manned and unmanned spacecraft.

This four-year project is expected to deliver a next-generation rad-hard space processor based on the ARM processor architecture to provide optimal power-to-performance for upgradeability, software availability, ease of use, and cost.

The HPSC project also will use Radiation Hard By Design (RHBD) standard cell libraries, as well as the ARM A53 processor with its internal NEON single instruction, multiple data (SIMD) design. Experts say a heterogeneous multi-core architectures using many different processor core types will not provide the best possible return on investment.

Applications for the HPSC processor will include military surveillance and weapons systems, human-rated spacecraft, habitats and vehicles, and robotic science and exploration platforms. System applications range from small satellites to large flagship-class missions.

Space computing tasks of the HPSC processor will include command and data handling, guidance navigation and control, and communications like software-defined radio; human assist, data representation, and cloud computing; high-rate real-time sensor data processing; and autonomy and science processing.

The software infrastructure for the HPSC Chiplet is envisioned to support both symmetric and asymmetric processing, and support both real-time operating systems and Unix/Linux based parallel processing. This infrastructure is also envisioned to support hierarchical fault tolerance, ranging from single Chiplet missions to multi-Chiplet highly redundant human missions. This software infrastructure is a contract deliverable.

Fault tolerance management middleware will enable the processor to detect and log errors; remove services likely to

experience hard failures; respond to uncorrectable errors; and implement n-modular redundancy, checkpoint/rollback, or other high-level fault tolerance.

This four-year project will consist of a preliminary design phase, a detailed design phase, a fabrication phase, and a test and characterization phase. The project should lead to a processor behavioral model, prototype processors, processor evaluation boards, and system software.

A key goal for the HPSC project is the ability to trade dynamically between processing throughput, power consumption, and fault tolerance. The HPSC processor architecture sometimes will be inside a dedicated spaceflight computer, and sometimes may be embedded in a science instrument or spaceflight subsystem.

Next Generation Space Processor (NGSP) study

Collaborative discussions with the Air Force Research Laboratory (AFRL) determined that many of NASA’s future onboard computing needs have commonality with the USAF’s future needs, and that a radiation-hardened, general purpose multi-core processor of the kind envisioned by NASA would also be relevant to the USAF.

Based on these shared interests, NASA partnered with AFRL on a Next Generation Space Processor (NGSP) study. This study, led by AFRL, engaged industry to assess, in greater detail, USAF’s requirements, compare USAF’s requirements with NASA’s previously defined detailed requirements, 3 develop processor architectures that would satisfy the superset of NASA/USAF requirements and evaluate these architectures against a set of government provided benchmarks.

The NGSP study provided the government team valuable guidance regarding the optimal architecture for a future spaceflight processing device:

– The use of COTS IP (specifically ARM based IP) provides optimal power-to performance, extensibility, evolvability, software availability, ease of use, and cost.

– The use of Radiation Hard By Design (RHBD) standard cell libraries provides required radiation tolerance.

– The augmentation of RHBD with higher-level fault tolerance techniques improves reliability.

– The use of the ARM A53 processor with its internal NEON Single Instruction, Multiple Data (SIMD) is sufficient for most near term applications.

– Heterogeneous multi-core architectures using multiple processor core types do not provide the optimum return on investment at this time.

– Architectural flexibility such as the ability to turn on/off cache coherency and use of L3 cache, as well as the ability to dynamically depower unused cores, including memory and Input/Output (I/O) interfaces, is useful to enable setting of optimal power: performance: fault tolerance operating point.

Radiation effects on Electronics and radiation hardening

Radiation has the potential to interfere with electronic devices and systems, creating so-called radiation-induced effects. Radiation effects on electronics are normally divided

into 3 different categories according to their effect on the electronic components:

Total ionizing dose (TID):

Total Ionizing Dose effects on modern integrated circuits cause the threshold voltage of MOS transistors to change because of trapped charges in the silicon dioxide gate insulator. For sub-micron devices these trapped charges can potentially “escape” by tunneling effects. Leakage currents are also generated at the edge of (N)MOS transistors and potentially between neighbor N-type diffusions. Commercial digital CMOS processes can normally stand a few Krad without a significant increase in power consumption. Modern sub-micron technologies tend to be more resistant to total dose effects than older technologies (in some cases up to several hundred Krad). High performance analog devices (e.g. amplifiers, ADC, DAC) may though potentially be affected at quite low doses. Total dose is measured in Rad or Gray (1 Gray = 100 Rad.)

Displacement damage:

Hadrons may displace atoms (therefore called displacement effect) in the silicon lattice of active devices and thereby affect their function. Bipolar devices and especially optical devices (e.g. Lasers, LEDs, Optical receivers, Opto-couplers) may be very sensitive to this effect. CMOS integrated circuits are normally not considered to suffer degradation by displacement damage. The total effect of different types of hadrons at different energies are normalized to 1 Mev Neutrons using the NIEL (Non Ionizing Energy Loss) equivalent.

Single event effects (SEE):

Single Event Effects refer to the fact that it is not a cumulative effect but an effect related to single individual

interactions in the silicon. Highly ionizing particles can directly deposit enough charge locally in the silicon to disturb the function of electronic circuits. Energetic Hadrons (> ~20Mev) can by nuclear interactions within the component itself generate recoils that also deposits sufficient charge locally to disturb the correct function. The different SEE effects are normally characterized by an energy threshold and a sensitivity cross-section at energies well above the threshold.

Single event upset (SEU):

The deposited charge is sufficient to flip the value of a digital signal. Single Event Upsets normally refer to bit flips in memory circuits (RAM, Latch, flip-flop) but may also in some rare cases directly affect digital signals in logic circuits.

Single event latchup (SEL):

Bulk CMOS technologies (not Silicon On Insulator) have parasitic bipolar transistors that can be triggered by a locally deposited charge to generate a kind of short circuit between the power supply and ground. CMOS processes are made to prevent this to occur under normal operating conditions but a local charge deposition from a traversing particle may potentially trigger this effect. Single event latchup may be limited to a small local region or may propagate to affect large parts of the chip. The large currents caused by this short circuit effect can permanently damage components if they are not externally protected against the large short circuit current and the related power dissipation.

Single event burnout (SEB):

Single event burnout refers to destructive failures of power MOSFET transistors in high power applications. For HEP applications this destructive failure mechanism is normally associated to failures in the main switching transistors of switching mode power supplies.

Radiation hard/tolerant design

For environments with high levels of radiation special technologies made to be immune to radiation must often be used (e.g. DMILL). Modern sub-micron CMOS technologies can often also be used in high radiation environments if special precautions are made in their design (e.g. enclosed transistors with guard rings).

Basically all CMOS technologies will be sensitive to single event upsets in their memory elements unless special schemes have been used. The general principles used to be insensitive to single event upsets is to use triple redundant logic and memories with error correcting codes (e.g. Hamming coding). Circuits with large memories and S-RAM based FPGAs should only be used in radiation environments after a careful analysis of single event upset problems.

The problem of single event burnout in power MOSFETs can in many cases be resolved by using a de-rating factor of ~2 of the main voltage and current limitations of the power transistor (implies redesign of power supply).

References and Resources also include:

“32-bit Radiation-Hardened Computers for Space,” Captains

Joseph Nedeau and Dan King, http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=687913

http://www.militaryaerospace.com/articles/2016/06/radiation-hardened-space-processor.html

https://www.fbo.gov/index?tab=documents&tabmode=form&subtab=core&tabid=6429a523ce641385373af828aec6794a

https://lhcb-elec.web.cern.ch/lhcb-elec/html/radiation_hardness.htm